Amendments to the Specification:

1) page 3, last paragraph, please replace this paragraph with the following amended text:

The invention [[detect]] detects fail bits of a DRAM cell during chip probe testing, in this manner saving test time and accurately detecting failing bits and providing a means for repairing the memory device at the time of chip probing. The column select (CSL) and word line (WL) pulses are under the instant invention self-time controlled, allowing ~~to emulate~~ emulating DRAM operation for different operating conditions.

2) page 9, last paragraph, page 10, first paragraph, please replace this paragraph with the following amended text:

This latter concern is further highlighted in the combined timing diagram that is shown in Fig. 3. Shown therein are the timing curves that previously have been highlighted and that therefore will not ~~need to~~ be ~~further~~ explained at this time. Key to the timing curves ~~that are~~ shown in Fig. 3 are the relative time frame in which these curves occur.

From this the concerns ~~that are~~ addressed by the invention can further be condensed into the curves ~~that are~~ shown in Figs. 4a and 4b, indicating that the invention addresses the period of time that the CSL pulse remains on (the duration of the CSL pulse), signal 38, Fig. 4a, and the time at which the WL pulse is turned off, signal 36, Fig. 4b.

The combination of these two aspects of the invention provides for the essential objective of the invention, that is to provide for an adjustable self-time scheme for write recovery for DRAM devices that operate at a speed which is considerably higher than the speed of the tester that is used to test the DRAM devices.